What is Claimed:

1. A charge coupled device made according to a standard CMOS process on a substrate of a first conductivity type, the charge coupled device comprising:

a dielectric layer overlaying at least a portion of the substrate, and

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes defining at least two charge wells, the at least two gate electrodes being separated by an inter-electrode gap; and

means for stabilizing the inter-electrode gap.

2. A charge coupled device according to claim 1, wherein the at least two charge well areas are formed in a semiconductor material of a first conductivity type and the means for stabilizing the inter-electrode gap includes a semiconductor region of the first conductivity type but having a different dopant concentration than the substrate, in the inter-electrode gap.

3. A charge coupled device according to claim 1, wherein the means for stabilizing the inter-electrode gap includes:

a further dielectric layer formed over the at least two gate electrodes; and

a further gate electrode formed overlying the further dielectric layer and positioned over the inter-electrode gap.

4. A charge coupled device according to claim 3, wherein the further dielectric layer is one of a gate oxide layer and a field oxide layer.

5. A charge coupled device according to claim 3, wherein the further gate electrode is formed from one of metal and polysilicon.

6. A charge coupled device according to claim 3, wherein the at least two charge well areas are formed in a semiconductor material of the first

conductivity type and the charge coupled device further includes a semiconductor region of the first conductivity type, formed in the semiconductor material beneath the inter-electrode gap, and having a different dopant concentration than the semiconductor material forming the at least two charge well areas.

7. A charge coupled device according to claim 1, wherein the means for stabilizing the inter-electrode gap includes means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause fringing fields from the at least two gate electrodes to extend into the inter-electrode gap.

8. A charge coupled device according to claim 1, wherein a first one of the charge well areas and its corresponding gate electrode form a photogate optical sensor and the charge coupled device further comprises:

a well region of a first conductivity type, adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

9. A charge coupled device according to claim 8, further including:

a further well region of the first conductivity type, the further well region forming a further charge barrier well; and

a plurality of further diffusion regions of the second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink and a plurality of transistors, wherein one of the at least two gate electrodes that is not a photogate overlies a portion of the further charge barrier well adjacent to the charge sink.

10. A charge coupled device according to claim 9, wherein the

plurality of transistors include a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

11. An optical sensor circuit for receiving photocarriers from a source and being formed on a single monolithic substrate comprising:

a charge coupled device (CCD) array, the array being formed of a plurality of pixels constructed with a standard single polysilicon CMOS process, each pixel including,

a first dielectric layer overlaying the substrate;

at least two gate electrodes overlaying the first dielectric layer and defining at least two charge wells, respectively, wherein adjacent ones of the at least two gate electrodes are separated by an inter-electrode gap, a combination of one of the at least two charge wells and its respective overlaying gate electrode forming a photogate optical sensor and a combination of another one of the at least two charge wells and its respective overlaying gate electrode forming a transfer gate; and

means for stabilizing the inter-electrode gap.

12. An optical sensor according to claim 11, wherein the at least two charge well areas are formed in a semiconductor material of a first conductivity type and the CCD array further includes a semiconductor region of the first conductivity type and having a different dopant concentration than the semiconductor material forming the at least two charge well areas, the further semiconductor region being formed in the semiconductor material, beneath the inter-electrode gap.

13. An optical sensor according to claim 11, further comprising:

a well region of the first conductivity type, adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first

conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

14. An optical sensor according to claim 13, further including:

a further well region of the first conductivity type, the further well region forming a further charge barrier well; and

a plurality of further diffusion regions of the second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink and a plurality of transistors, wherein one of the at least two gate electrodes that is not a photogate overlies a portion of the further charge barrier well adjacent to the charge sink.

15. A charge coupled device according to claim 13, wherein the plurality of transistors include a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

16. An imager system comprising:

a single monolithic integrated circuit including:

a charge coupled device (CCD) imager array; and

a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array.

17. A camera system comprising:

a single monolithic integrated circuit including:

a charge coupled device (CCD) imager array; and

a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array; and

optics configured to focus radiation onto the CCD imager array.

18. A charge coupled device made according to a standard single polysilicon CMOS process, the charge coupled device comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type, opposite to the first conductivity type;

an oxide layer formed over at least the well region;

first and second polysilicon gate electrodes formed on the oxide layer over the well region, the first and second gate electrodes being separated by an inter-electrode gap, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register.

19. A charge coupled device made according to a standard single polysilicon CMOS process, the charge coupled device comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type, opposite to the first conductivity type defining a channel;

at least one diffusion of the first conductivity type in a portion of the well region

an oxide layer formed over the well region and the at least one diffusion;

first and second polysilicon gate electrodes formed on the oxide layer over a portion of the well region, exclusive of the at least one diffusion, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a virtual gate CCD register.

20. A back illuminated imager comprising:

a substrate of a first conductivity type having a front side and a back side;

a photodetector formed in the front side of the substrate;

a well region of a second conductivity type, opposite to the first conductivity type, formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction; and

at least one diffusion region in the well region of the second conductivity type forming a component of the back illuminated imager;

whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction.

21. An electronic camera system comprising:

an imager formed according to one of claims 18, 19 and 20; and

optics that are configured to focus radiation onto the imager.

22. A method of making a charge coupled device (CCD) register using a standard complementary metal oxide semiconductor (CMOS) process comprising the steps of:

providing a substrate of a first conductivity type;

forming an oxide layer over the substrate;

forming first and second polysilicon electrodes over the oxide layer, the first and second polysilicon electrodes being separated by an inter-electrode gap and defining a channel; and

stabilizing the inter-electrode gap.

23. A method of making a CCD register according to claim 22, wherein the step of stabilizing the inter-electrode gap includes the step of forming a semiconductor region of the first conductivity type but having a different dopant concentration than the substrate.

24. A method of making a CCD register according to claim 22, wherein the step of stabilizing the inter-electrode gap includes the steps of:

forming a further dielectric layer over the at least two gate electrodes; and

forming a further gate electrode overlying the further dielectric layer and positioned over the inter-electrode gap.

25. A method of making a CCD register according to claim 22, wherein the step of stabilizing the inter-electrode gap includes the step of applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause fringing fields from the at least two gate electrodes to extend into the inter-electrode gap.

26. A method of making a CCD register according to claim 22, further including the step of forming a well region of a second conductivity type, opposite to the first conductivity type in the substrate before forming the oxide layer, the well region being configured to be beneath the first and second polysilicon electrodes to form a buried channel structure.

27. A method of making a CCD register according to claim 22, further including the step of forming a barrier well region as a well region of the first conductivity type and a diffusion region of the second conductivity type, inside the barrier well region as a blooming drain, the diffusion region of the second conductivity type having a higher dopant concentration than the barrier well region.

28. A method of making a CCD register according to claim 22, further including the step of forming a further barrier well region of the first

conductivity type and a plurality of further diffusion regions of the second conductivity type, inside the further barrier well region, the plurality of further diffusion regions of the second conductivity type having a higher dopant concentration than the barrier well region and forming source and drain electrodes of the at least one transistor.

29. A method for making a back illuminated imager array comprising the steps of:

providing a substrate of a first conductivity type, the substrate having a front surface and a back surface;

forming a photodetector in the front surface of the substrate;

forming a well region of a second conductivity type, opposite to the first conductivity type in the front surface of the substrate;

forming at least one imager component in the well region;

thinning the imager by removing a portion of the substrate from the back side of the substrate; and

annealing the thinned imager.

30. A method according to claim 29 further including the step of applying a refractory metal as a metalization layer to the at least one imager component prior to thinning the imager.